REMARKS

This is in response to the Final Office Action of July 15, 2004. Claims 32-67 were rejected. Claims 32 and 55 were amended. Claims 32-67 are pending.

In the Final Rejection the Examiner repeated the rejections that were made in the previous Office Action. In the Amendment of March 25, 2004, Applicant pointed out that the cited references, Nielsen and Aleksic, teach away from Applicant's invention of a graphics subsystem because the cited references disclose a unified memory architecture that stores both system data and graphics data in a common memory. In section 4 of the Final Rejection, the Examiner rejected this argument, stating that the Examiner interpreted the claims to read on Nielsen and Aleksin. It is Applicant's understanding that the Examiner contends that the claim limitations corresponding to a "graphics subsystem" and a "graphics memory" do not adequately distinguish over a UMA architecture that stores both graphics data and system data in a common memory.

Applicant has therefore amended independent claims 32 and 55 to recite limitations specific to a dedicated graphics system having a plurality of different graphics processing units. The independent claims were amended to clarify that individual memory requests from the graphics processing units have an associated data transfer size. Additionally, the independent claims were amended to clarify that data requests not requiring all of the memory partitions may be serviced in parallel via different partitions to improve throughput. Support for these limitations are found on page 2, line 28 to page 3, line 30.

One benefit of Applicant's claimed invention is that throughput and fetching efficiency are improved in a graphics system. In conventional graphics systems having a non-partitioned memory, the memory access size is selected to accommodate the need of the graphics system to transfer large amounts of data. However, the size of individual data transfers may vary. In some cases the entire memory bus bandwidth may be required but in other cases the entire bandwidth is not required and hence is wasted. As a result, memory is used inefficiently whenever individual graphics processing units request memory transfers that do not require the full memory bus bandwidth. For example, consider the case of a small geometry object having a small number of pixels.

For the case of a small geometry object, individual graphics processing units may require data transfers that are smaller than the full memory bus bandwidth. As discussed on page 1, line 29 to page 2, line 10, in a conventional graphics system a "fetching efficiency" is defined as the ratio of pixels used for a geometry object to the pixels fetched during an access. A small ratio implies wasted memory throughput. In a conventional non-partitioned memory the fetching efficiency decreases if the memory bus size increases.

Applicant's claimed invention permits variable transfer size data requests to be efficiently serviced. For example, Applicant's invention permits data requests having a large data transfer size to be serviced using all of the partitions, if necessary. However, in Applicants invention, the partitions are independently accessible. If a particular memory request does not require all of the partitions, the other partitions are free to be used by the memory controller to service other requests, as described on page 3, lines 25-30. As a result, the throughput is improved.

The cited references do not teach or suggest a partitioned memory in which a determination is made if an individual memory request not requiring all of the partitions can be serviced in parallel with another request using a different subset of partitions to improve throughput. Nielsen discloses a unitary (non-partitioned) memory architecture that does not permit memory accesses to be performed in parallel using a different subset of partitions. Aleksic discloses a unitary memory system having a memory controller that accesses two channels of memory (CH1 and CH0). Graphics data requiring 128 bits is accessed either by accessing both channels simultaneously or by accessing the channels separately and buffering the data until the full 128 bit data word is available, as described on column 7, line 63 to column 8, line 2. However, there is no teaching or suggestion in Aleksic that individual requests have a variable data transfer size. Moreover, there is no teaching or suggestion in Aleksic that two or more small data requests from different graphics clients are serviced in parallel via different partitions to improve throughput. Consequently, Applicant respectfully submits that the cited references fail to teach or suggest several limitations of Applicant's claimed invention.

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is now in condition for allowance. The Examiner is invited to contact

the undersigned if there are any residual issues that can be resolved through a telephone call.

The Commissioner is hereby authorized to charge any appropriate fees to Deposit Account No. 03-3117.

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Respectfully submitted,
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